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(19) **United States**(12) **Patent Application Publication****Terzioglu et al.**(10) **Pub. No.: US 2007/0109886 A1**(43) **Pub. Date: May 17, 2007**(54) **BLOCK REDUNDANCY IMPLEMENTATION  
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**Chicago, IL 60661 (US)**(21) Appl. No.: **11/616,573**(22) Filed: **Dec. 27, 2006****Related U.S. Application Data**(63) Continuation of application No. 10/729,405, filed on  
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6,411,557.**Publication Classification**(51) **Int. Cl.**  
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(52) **U.S. Cl.** ..... **365/200**(57) **ABSTRACT**

The present invention relates to a system and method for providing redundancy in a hierarchically memory, by replacing small blocks in such memory. The present invention provides such redundancy (i.e., replaces such small blocks) by either shifting predecoded lines or using a modified shifting predecoder circuit in the local predecoder block. In one embodiment, the hierarchal memory structure includes at least one active predecoder adapted to be shifted out of use; and at least one redundant predecoder adapted to be shifted in to use.

